

Attorney's Docket No.: 10559-177001
Assignee: Intel Corporation
Client's Ref. No.: P8237

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Applicant: Kalpesh Mehta Art Unit : 2126
Serial No.: 09/771,374 Examiner : Li Zhen
Filed: January 26, 2001 Assignee: Intel Corporation

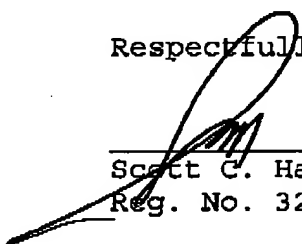
Title : APPORTIONING A SHARED COMPUTER RESOURCE

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Brief on Appeal and Petition for Extension of Time faxed this
27th day of June, 2005, to the United States Patent and Trademark
Office.

Respectfully submitted,

Date: June 27, 2005



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Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BRIEF ON APPEAL

Sir: Applicant herewith files this brief on appeal under 37 CFR 41.37, thereby perfecting the notice of appeal which was originally filed on April 19, 2005. The sections required by Rule 41.37 follow.

(1) Real Party in Interest

The case is assigned of record to Intel Corp., who is hence believed to be the real party in interest.

(2) Related Appeals and Interferences

There are no known related appeals and/or interferences.

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(3) Status of Claims

Claims 4, 5, 9-10, 14-20 are pending and are rejected.

Claims 1-3, 6-8 and 11-13 have been previously canceled.

(4) Status of Amendments

An amendment after final was filed on January 20, 2005, and was indicated as being entered in an advisory action mailed April 5, 2005 (paper number 20050330).

(5) Summary of Claimed Subject Matter

Claim 18 defines a method which allows computer processes to be assigned with both an access value and a priority value. Each of the plurality of computer resources is assigned an access value (page 3 lines 26-27), and a priority value (page 4 lines 10-12). The priority value can be either high or low priority see page 4 lines 11-12. During a first access cycle, access is provided to processes first whose access value represents high priority and whose access value represents the access should still be granted. See generally page 4 lines 23-30. The access values may be reallocated after each cycle, see page 5 lines 15-17.

Claim 18 requires determining that all priority high requests have access values that indicate no additional access

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should be granted see page 5 lines 1-5. After that determining, access is provided to the low priority requests see page 5 line for-19. After both the high and low requests have been given access, a new cycle is started, see page 5 line 26 through page 6 line 2.

Claim 19 defines assigning an access value and a priority value (page 3 lines 26-27 and page 4 lines 10-12). Claim 19 defines that access during the first access cycle access is first provided to the high priority processes and the access value is adjusted, page 4 lines 23-30; page 5 lines 15-17. Claim 19 defines providing access to the low priority requests after that, page 5 lines 4-19 and starting a new cycle after both high and low requests have been granted, see page 5 line 26 through page 6 line 2.

Claim 20 defines a controller with ports, including ports for connecting to different processes see generally page 3 lines 7-9. Claim 20 defines a memory 130, see page 3 line 9. The memory stores access values see page 3 lines 18-20. The controller operates to assign an access value and a priority value to the computer resources (page 3 lines 26-27 and page 4 lines 10-12) provides accesses to the high priority values first, (page 4 lines 23-30) reallocates those values (page 5 lines 15-17) after that provides access to the low priority

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requests (page 5 lines 4-19) and then starts a new cycle (page 5 line 26 through page 6 line 2).

(6) Grounds of Rejection

The single ground of rejection for review on appeal is whether claims 4, 5, 9, 10 and 14-20 are properly rejected under 35 USC 103 as being unpatentable over Hedge in view of Schaffer, et al.

(7) Argument

Claim 18 defines bandwidth allocation as well as access priority to a plurality of computer processes that request access to a shared resource. Claim 18 defines providing access to the high priority values. After those values obtain access, access is provided to the lower priority access values. Importantly, claim 18 also defines, after granting each access, "adjusting an access value associated with the access".

The examiner and the undersigned differ strongly on their interpretation of prior art. The examiner has taken an interpretation of the prior art which, with all due respect, turns the prior art on its head in order to meet the limitations of the claims.

Admittedly, Hedge teaches a system with priority and

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bandwidth allocation. However, note that Hedge is entirely different than the present claims, and the interpretation made of this prior art is inconsistent. The present claims require that all of the high priority processes are given access, then all the low priority processes are given access (emphasis added). This requires multiple processes, which is not met by the present interpretation. In this way, everything gets access in any one cycle. Hedge is entirely different, since it defines a "preemptive priority" environment, see generally column 5 line 53. As explained in that paragraph, a higher priority process preempts the currently executing process without waiting for it to give up the CPU. In contrast, claim 18 defines an entirely different way of operating. According to claim 18, high priority processes are executed first, low priority second. There is no way to preempt the priority. As explained in detail in Hedge, a running tally of bandwidth percentage is maintained, see column 6 lines 57-67. The bandwidth manager evaluates the count values at each cycle. Once the process has used its allocated bandwidth, then other processes get priority until they have used their allocated bandwidth. This has the effect of allocating the bandwidth, but does in an entirely different way than that which is claimed. That is, according to Hedge, the table is used to determine which process gets the next

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"tick" of CPU bandwidth, based on that tally. According to claim 18, all the high priority processes get access first, then all the low priority processes. There is no access to a table.

Claim 18 also defines that the access priority "can be high priority or low priority". This is entirely inconsistent with Hedge which assigns analog values to the priority, rather than simply high and low.

Claim 18 also defines an access cycle. Hedge teaches nothing about an access cycle, but rather continually monitors values in the table. Claim 18 requires that after both high priority requests and low priority requests when each have access values that represent no further access, new access values are set. Hedge has no analogue of this feature, since it teaches nothing about an access cycle. Rather, Hedge continually monitors that table as previously discussed. Claim 18 hence defines a time period within which the values must all be satisfied. During the first access cycle, first access is provided to the high priority processes, then to the low priority processes, until each of those processes has been granted access. Then, the values are reassigned.

This is an entirely different system than Hedge who simply maintains a percentage value in a table, and accesses the table to determine which processes entitled to the next bit of

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storage. There is no "starting a new access cycle with new values" in Hedge.

The above has extensively described Hedge. It is noted that the rejection now is based on Hedge in view of Shaffer. However, the rejection of claim 18 only referred to Hedge. To the extent that Shaffer is attempted to be combined with Hedge, it is respectfully suggested that the hypothetical combination still would not render obvious claim 18. Shaffer teaches a computer system with an arbitration system that controls relative dynamic priority of each request. See generally column 5 lines 28-column 6 line 5. Shaffer teaches who obtains bus access at a given time. It does not teach or suggest the subject matter discussed above.

Claim 19 should be allowable for analogous reasons to those discussed above. Hedge in view of Schaffer, et al. does not teach:

assign an access value and a priority value where the priority value can be high priority or low priority.

During a first access cycle, satisfying all the high priority access first, then satisfying all the low priority accesses, then starting a new access cycle with new access values and new priority values. Hedge simply teaches maintaining percentage values in the table.

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Claim 20 should be allowable for analogous reasons, as it defines an access value and a priority value, the concept of an access cycle, and the other similar advantageous features discussed above.

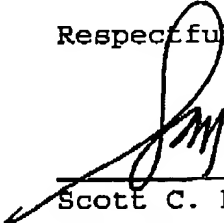
Each of the dependent claims should be allowable by virtue of their dependency, as well as on their own merits.

In view of the above, it is respectfully suggested that all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply the brief fee of \$500 and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 6/27/05



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Appendix of Claims

4. The method according to claim 18 wherein at least one of the computer processes is an isochronous process.

5. The method according to claim 18 wherein at least one of the computer processes is an asynchronous process.

9. The technique according to claim 19 wherein at least one of the computer processes is an isochronous process.

10. The technique according to claim 19 wherein at least one of the computer processes is an asynchronous process.

14. The apparatus according to claim 20 wherein at least one of the computer processes is an isochronous process.

15. The apparatus according to claim 20 wherein at least one of the computer processes is an asynchronous process.

16. The apparatus according to claim 20 wherein the controller device is a memory controller.

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17. The apparatus according to claim 20 wherein the shared memory resource is a shared memory bank.

18. A method, comprising:

assigning an access value and a priority value to each of a plurality of computer processes which request access to a shared computer resource, where the priority value can be high priority or low priority;

during an first access cycle, first providing access to processes whose access value represents high priority and whose access value represents that access should still be granted during the access cycle, and after granting each access, adjusting an access value associated with said each access, to indicate that additional access has been granted;

determining, during said first access cycle, that all high priority requests have access values that indicate that no additional access should be granted;

responsive to said determining, in said first access cycle, providing access to low priority requests whose access values represent that access should be granted, and adjusting access values after granting the access; and

after determining that both the high priority requests and low priority requests each have access values that represent no

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further access should be granted in said first access cycle, starting a new access cycle with new access values and priority values.

19. An article comprising a computer readable media which stores executable instructions for controlling access to a shared computer resource by at least two computer processes, the instructions, when executed, causing the computer to:

assign an access value and a priority value to each of a plurality of computer processes which request access to a shared computer resource, where the priority value can be high priority or low priority;

during a first access cycle, first provide access to processes whose access value represents high priority and whose access value represents that access should still be granted during the access cycle, and after granting each access, adjust an access value associated with said access to indicate that additional access has been granted;

determine, during said first access cycle, that all high priority requests have access values that indicate that no additional access should be granted;

responsive to said determining, in said first access cycle, provide access to low priority requests whose access values

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indicate that access should be granted, and adjust access values after granting the access; and

after determining that both the high priority requests and low priority requests each have access values that represent no further access should be granted in said first access cycle, start a new access cycle with new access values and priority values.

20. An apparatus, comprising:

a controller device, having a first port for connecting to a shared resource, and at least one second port for connecting to a plurality of different processes which are requesting access to the shared resource,

a memory operating to store access values,

said controller operating to:

assign an access value and a priority value to each of a plurality of computer processes which request access to a shared computer resource, where the priority value can be high priority or low priority, and store said values in said memory, during a first access cycle, first controlling said processes to provide access to processes whose access value represents high priority and whose access value represents that access should still be granted during the access cycle, and after granting

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each access, adjusting an access value associated with said access to indicate that additional access has been granted, determining, during said first access cycle, that all high priority requests have access values that indicate that no additional access should be granted, responsive to said determining, in said first access cycle, providing access to low priority requests whose access values represent that access should be granted, and adjusting access values after granting the access; and

after determining that both the high priority requests and low priority requests each have access values that represent no further access should be granted in said first access cycle, starting a new access cycle with new access values and priority values.